REMARKS

Claims 1-24 are pending in the application, of which claims 1, 6, 11, 16, and 22 are independent. The applicant has amended claims 1, 6, and 11 and canceled claims 4 and 9. Favorable reconsideration and further examination are respectfully requested.

The examiner objected to the specification. The applicant has amended the specification and so this objection should be withdrawn.

The examiner rejected claims 1, 6, and 11 under 35 U.S.C. 112 as being indefinite for failing to point out and distinctly claim the subject matter the applicant regards as his invention. Applicant disagrees. Use of the definite article "the" in the claims (i.e., use of the phrase "a node" followed by the phrase "the node") distinctly defines the metes and bounds of the claims such that one of skill in the art would be able to understand the scope of the claim.

The Examiner rejected claims 1-15 under 35 U.S.C. 103(a) as being unpatentable over Jain (US 6,044,211) in view of Butts (5,734,581).

Claim 1 relates to a method of simulating a logic design. The method includes storing a first state, a second state, and a third state and performing a three state simulation of the logic design to determine an output of the node in simulation based on the first state, the second state, and the third state. The method also includes determining if the simulation of the logic design was successful based on whether the output of the node has an undefined state and performing four state simulation of the logic design if the three state simulation of the logic design was successful. Jain neither describes nor suggests Claim 1 whether taken alone or in combination with Butts.

The examiner states that Jain discloses performing a simulation of a logic design based on stored values of prior states and that Jain does not explicitly disclose three distinct state values. The examiner relies on Butts to teach multi-state simulation using three logic states. While Butts discloses representing "more than two states of a logic signal in a logic simulation environment" (see Col. 67, lines 32-37), this teaching does not suggest the features of claim 1. That is, Butts fails to disclose a four state simulation of the logic design performed if the three state simulation of the logic design was successful.

Claims 6 and 11 include similar limitations to claim 1 and are patentable for at least the reasons discussed in relation to claim 1. For at least the same reasons, applicant submits claims 1, 6, and 11 should be allowed, applicant submits that dependent claims 2-5, 7-10, and 12-15 should also be allowed.

The Examiner rejected claims 16-21 under 35 U.S.C. 102(b) as being unpatentable over Marino (4,587,625).

Claim 16, as amended, includes "storing three bits of state information for a node included in a logic design, , where the state information is represented by one of two possible values of the three bits of state information as a first bit of the three bits representing the presence or absence of a high state for the node, a second bit of the three bits representing the presence or absence of a logic low state for the node, and a third bit of the three bits representing the presence or absence of an undefined state based for the node."

Marino represents the state of each location or node "by a three-bit word having five permitted values" (col. 2, lines 20-22). As shown in table one in column 3, a particular combination of the three bits is used to indicate the state of the node. For example, the combination "000" represents a low level while the combination "001" represents a high level. As shown in table 1 (Marino Col. 3, lines 50-55), it is the combination of the three bits and not the value of a particular bit that indicates a state of the node. Therefore, Marino fails to disclose or suggest storing only three bits of state information for a node included in a logic design where a first bit of the three bits represents the presence or absence of a high state for the node, a second bit of the three bits represents the presence or absence of a logic low state for the node, and a third bit of the three bits represents the presence or absence of an undefined state based for the node as in the applicant's claim 16.

For at least the same reasons, applicant submits claim 16 should be allowed, applicant submits that dependent claims 17-21 are also allowable.

The Examiner rejected claims 22-25 under 35 U.S.C. 103(a) as being unpatentable over Chan (US 6,466,898) in view of Wang (6,738,875).

Claim 22 relates to a method for simulating a logic design using cycle based simulation. The method includes attempting to write a result of a logic computation instruction to a first memory page storing an original value, the memory page being write protected copying the instruction in a second memory page, executing the second memory page starting with the instruction, unprotecting the write protected memory page and storing a result of the instruction at the location in the write protected memory page, rewriting the original value to the location in the write protected memory page if the original value differs from the result, and re-protecting the write protected memory page. Chan neither describes nor suggests claim 22 whether taken alone or in combination with Wang.

The examiner states that Chan does not explicitly disclose a write protected memory. The examiner also states that Wang teaches "techniques for write protecting a memory page, copying to secondary pages, un-protecting a write-protected page, rewriting values, and reprotecting the original write protected page" in column 1, line 55 to column 2, line 7. Applicant disagrees. In column 1, line 55 to column 2, line 7, Wang teaches unprotecting a write protected page in response to a page fault such that the page can be accessed by the application. Wang fails to disclose or suggest "copying the instruction in a second memory page" and "executing the second memory page starting with the instruction" as in the applicant's claim 22.

For at least the same reasons, applicant submits claim 22 should be allowed, applicant submits that dependent claims 23-24 should also be allowed.

Applicant requests that the examiner initial the information disclosure form filed in December 2003. The examiner has signed the 1449, but has not initialed the six references cited on the form.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this

paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 3/3/05

Denis G. Maloney
Reg. No. 29,670

Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

21035908.doc